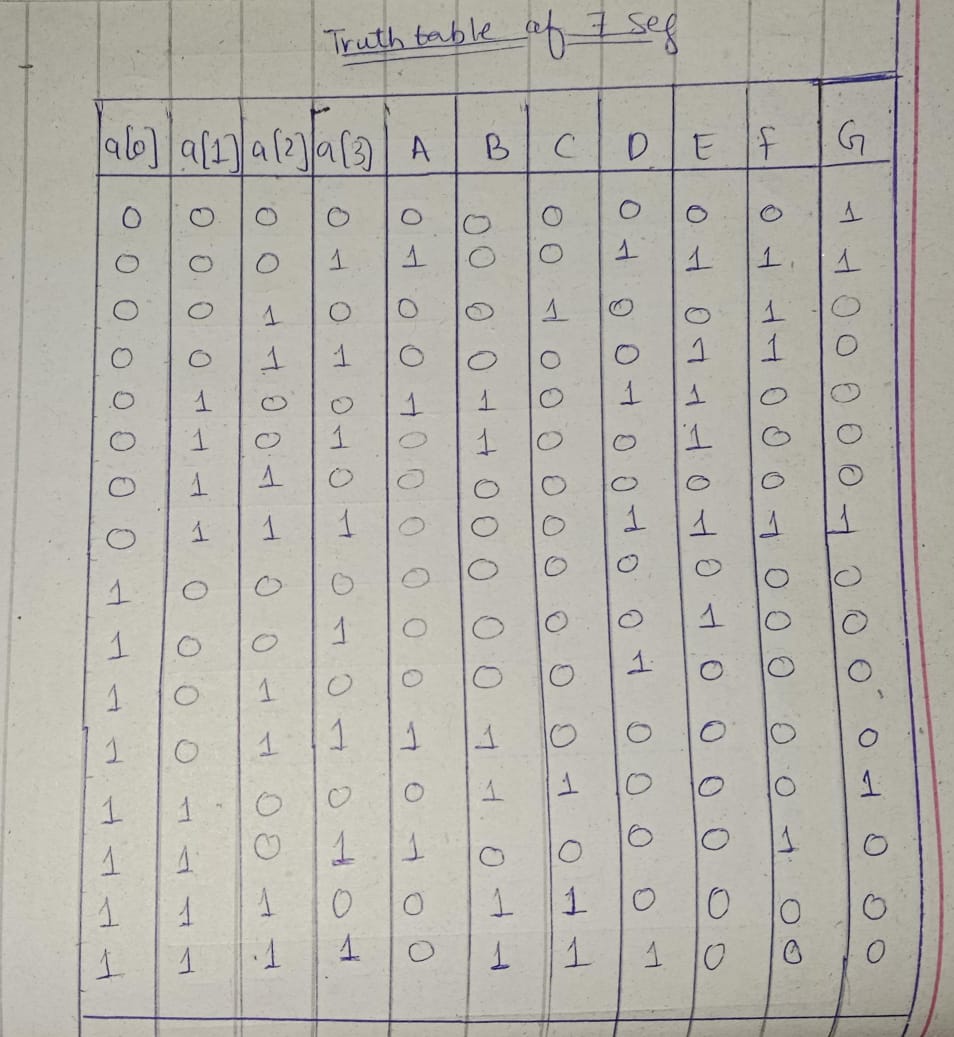
**Ayesha Sajjad 2022-EE-107**

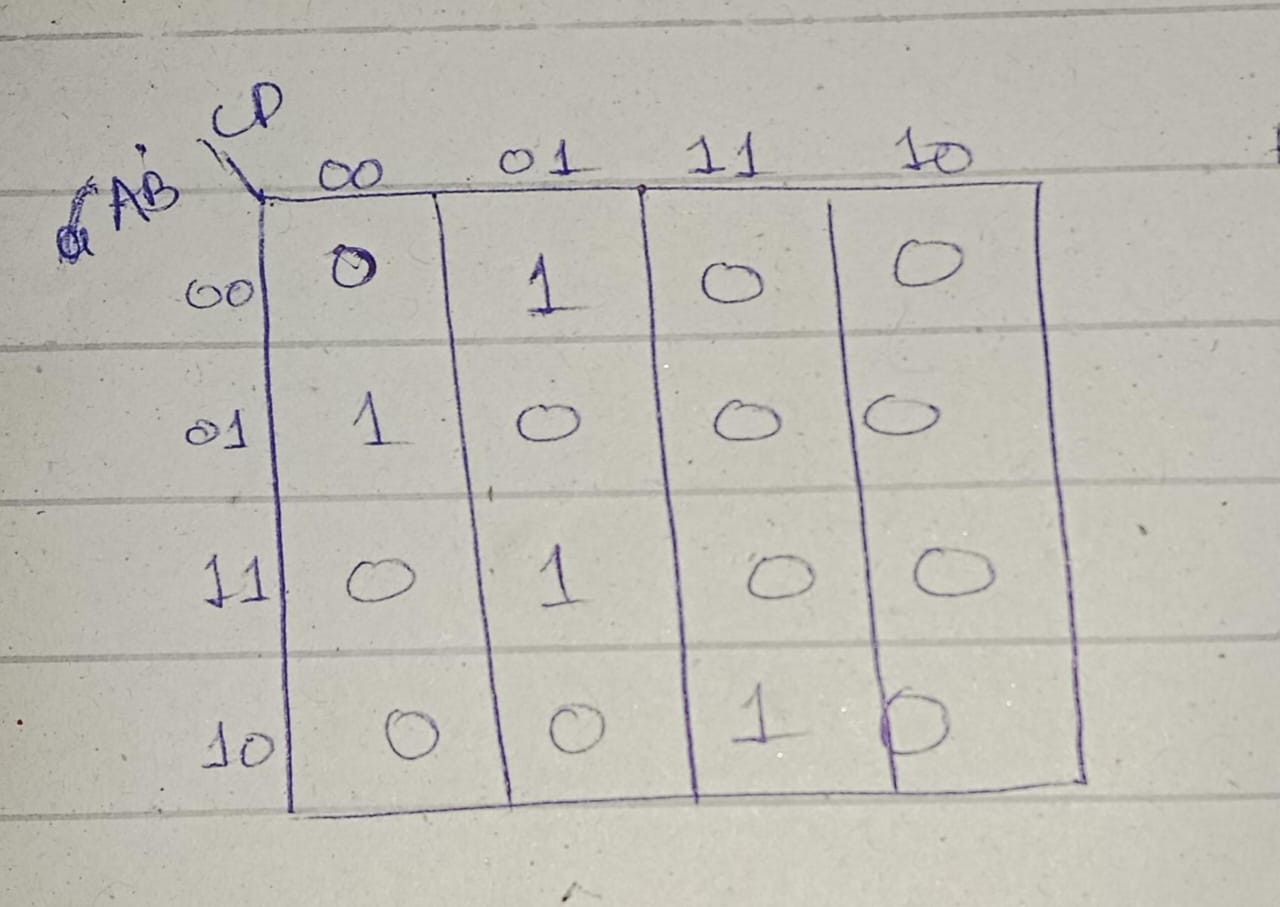
**Experiment 5**

**Combinational Circuit Design: Seven Segments Display using K-Maps**

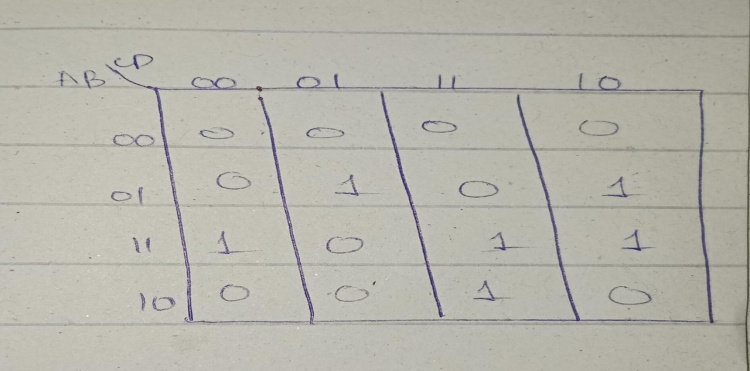
**Truthtable for 7 segment display:**

****

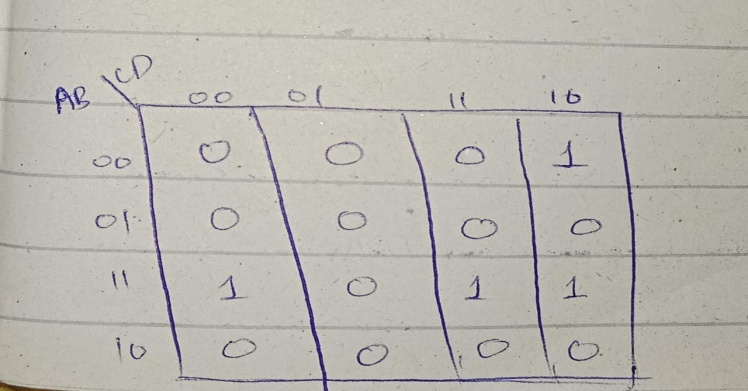
**K map for A:**

****

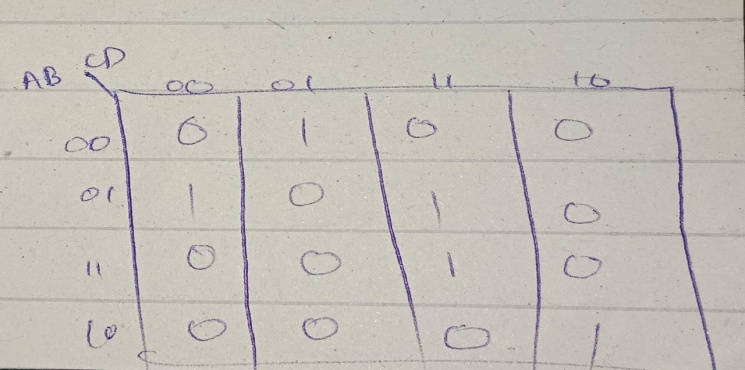
**K Map for B:**

****

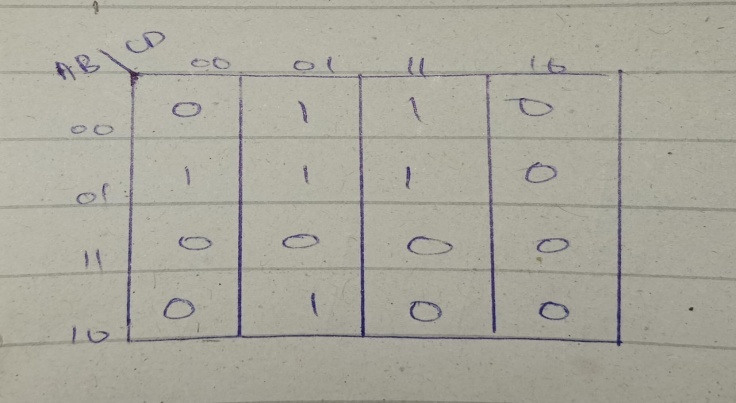
**K map for C:**

****

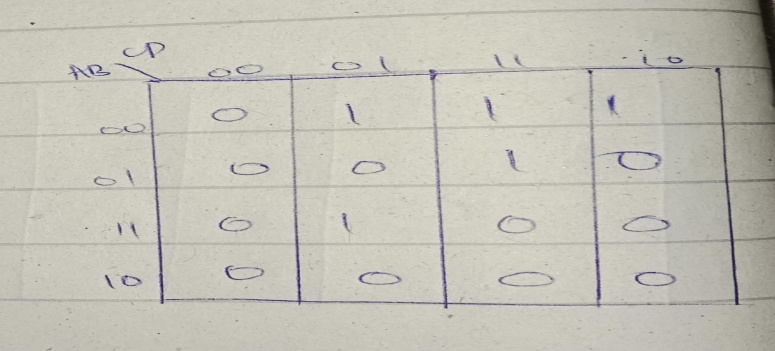
**K map for D:**

****

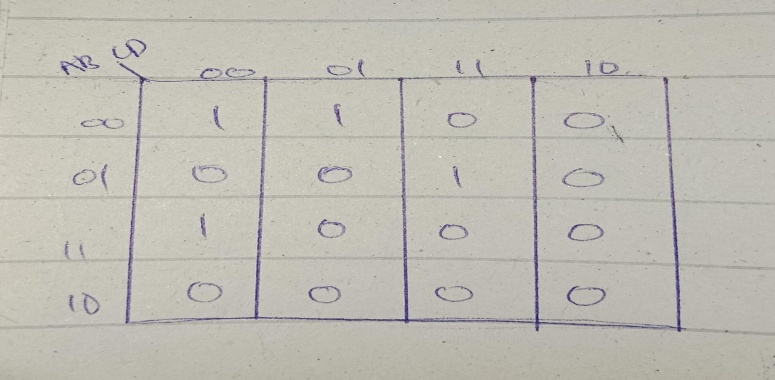
**K map for E**

**:**

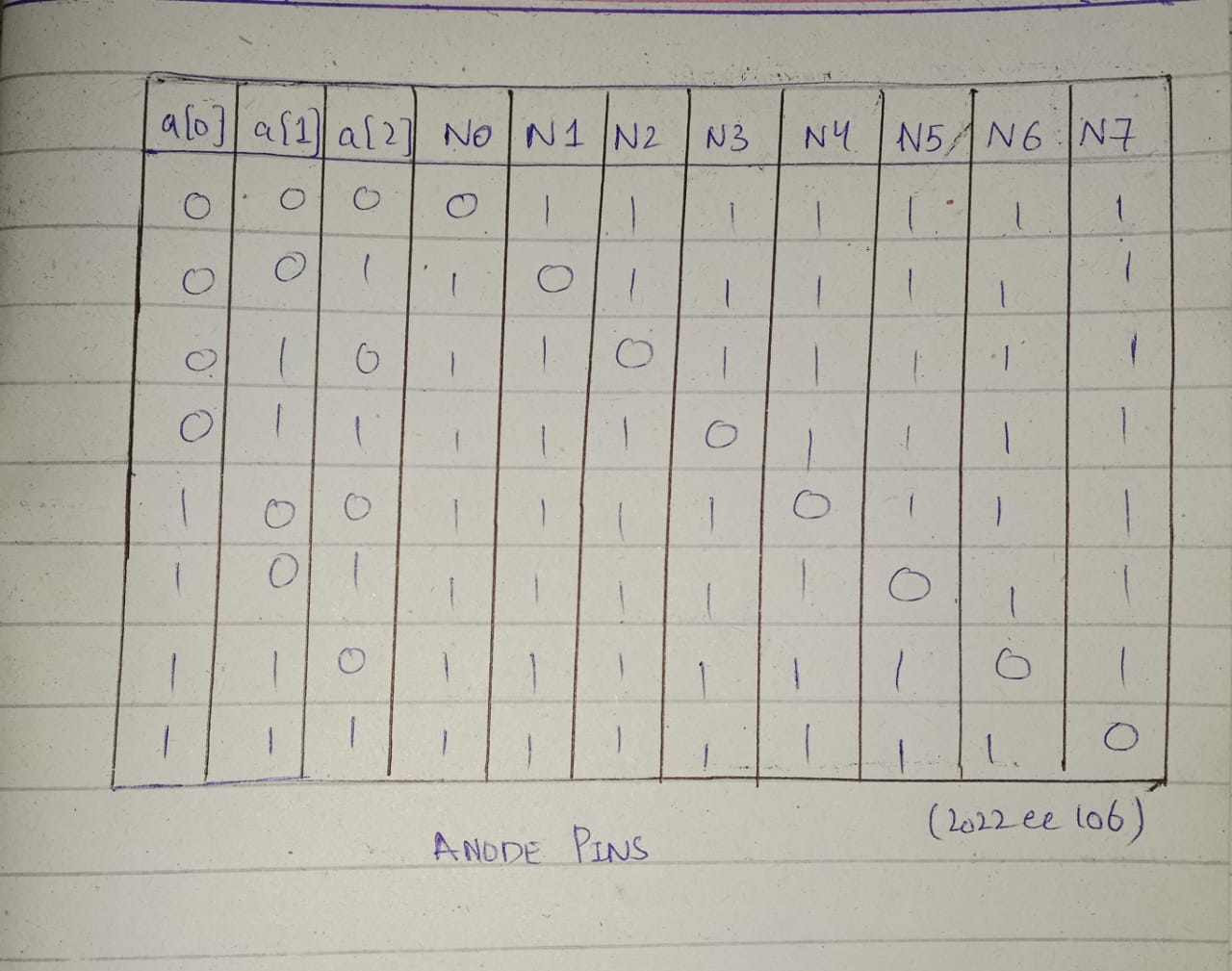
**K map for F:**

****

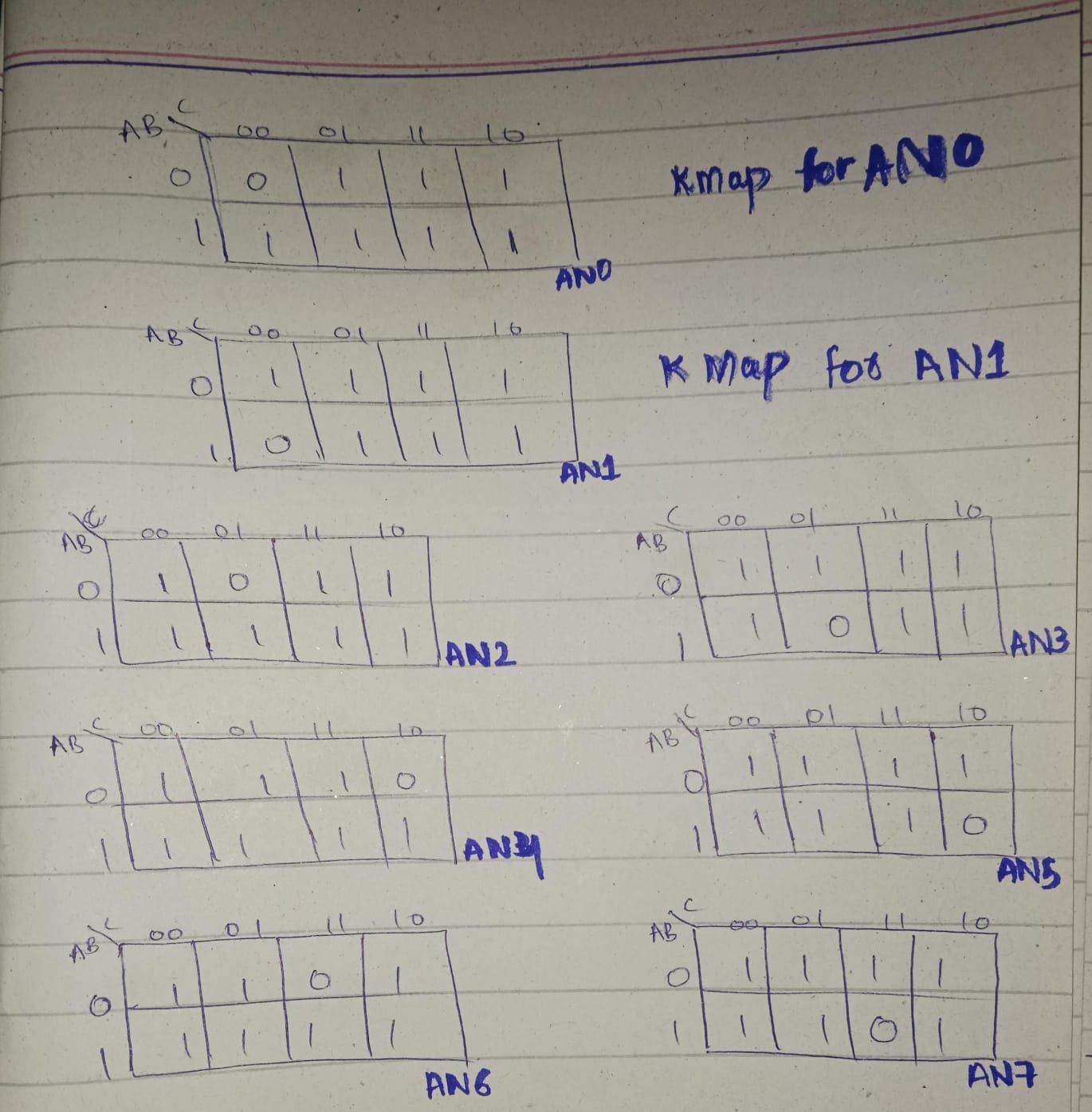
**K map for G:**

****

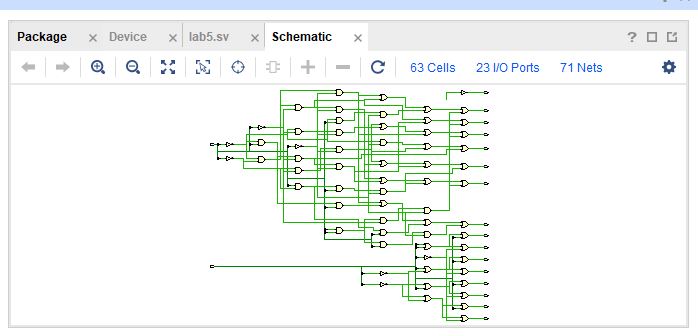
**Truthtable for anode pins:**

****

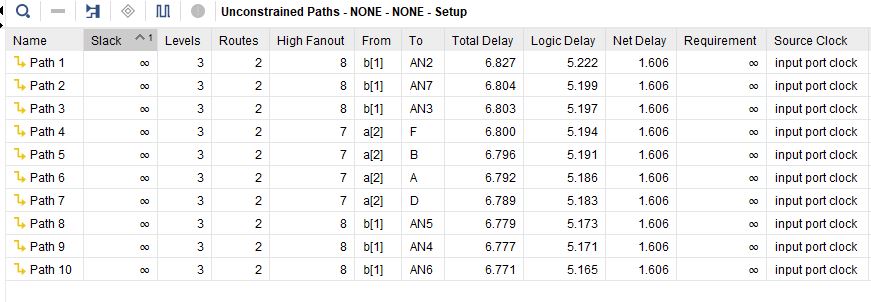
**K map :**

****

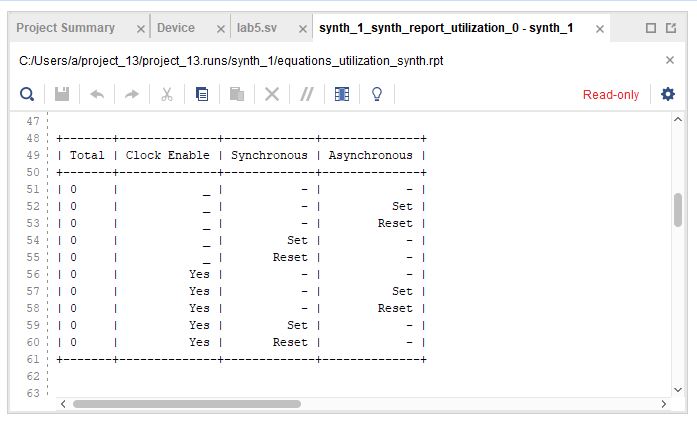
**Circuit diagram inferred by the Xilinx Vivado:**

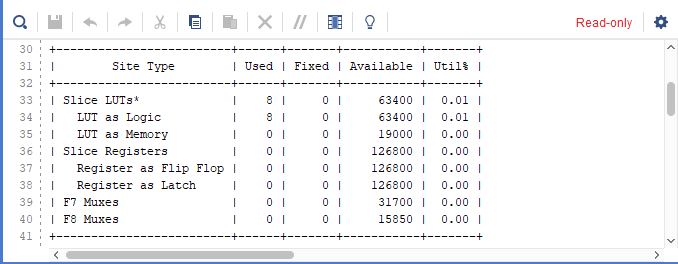
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**Combinational delay:**

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**Resource Utilization Summary:**

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